

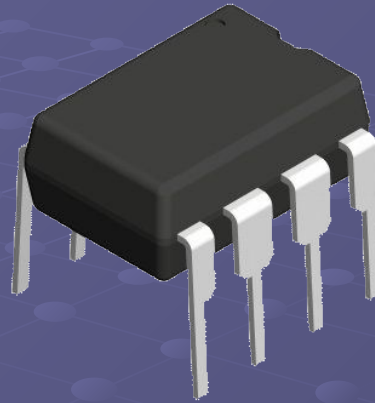
Programmable logic and FPGA

CPU Architecture

Objectives

- What is a programmable logic
- What is an FPGA
 - Structure
 - Special functions
 - Comparison and Usages
- Altera Cyclone II 20 FPGA
- Design Flow

Semiconductor Chips



ASICs

Application Specific
Integrated Circuits

Microprocessor
s

Microcontrollers

FPGA & CPLD

Programmable logic

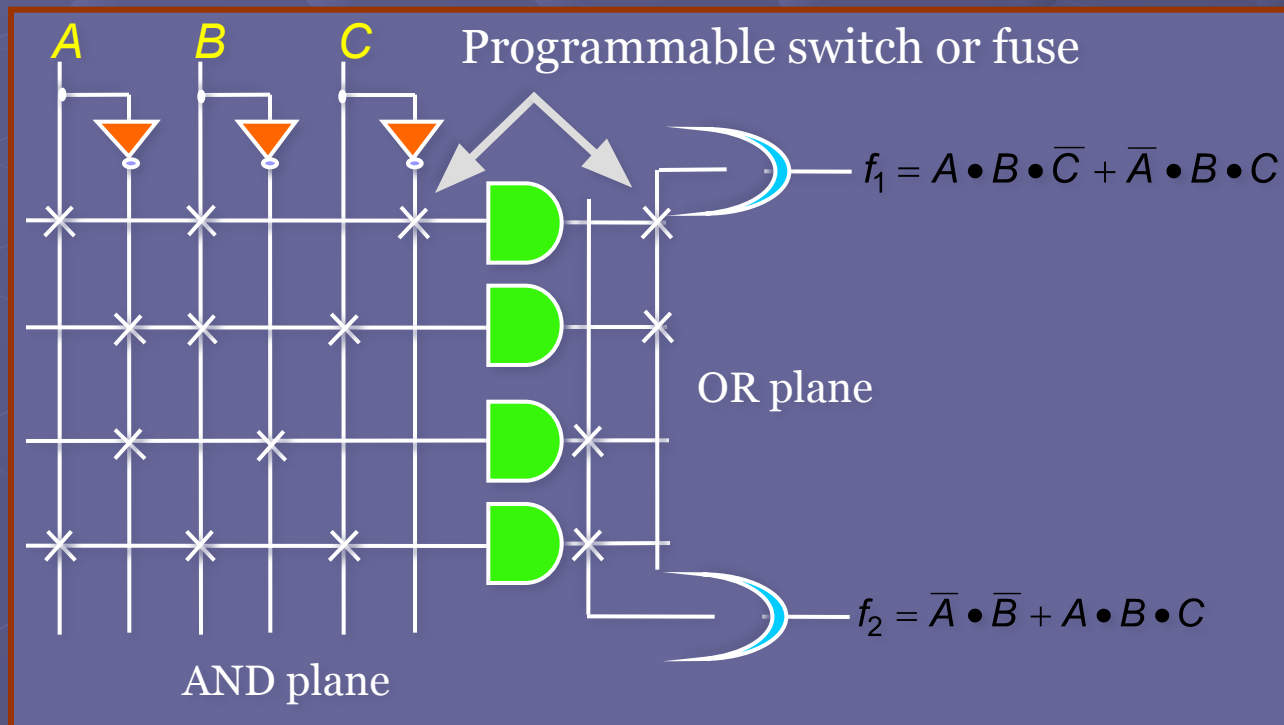
- An integrated circuit that can be programmed/reprogrammed with a digital logic of a certain level.
- Started at late 70s and constantly growing
- Now available of up to approximately 700K Flip-Flops in a single chip.

Advantages

- Short Development time
- Reconfigurable
- Saves board space
- Flexible to changes
- No need for ASIC expensive design and production
- Fast time to market
- Bugs can be fixed easily
- Of the shelf solutions are available

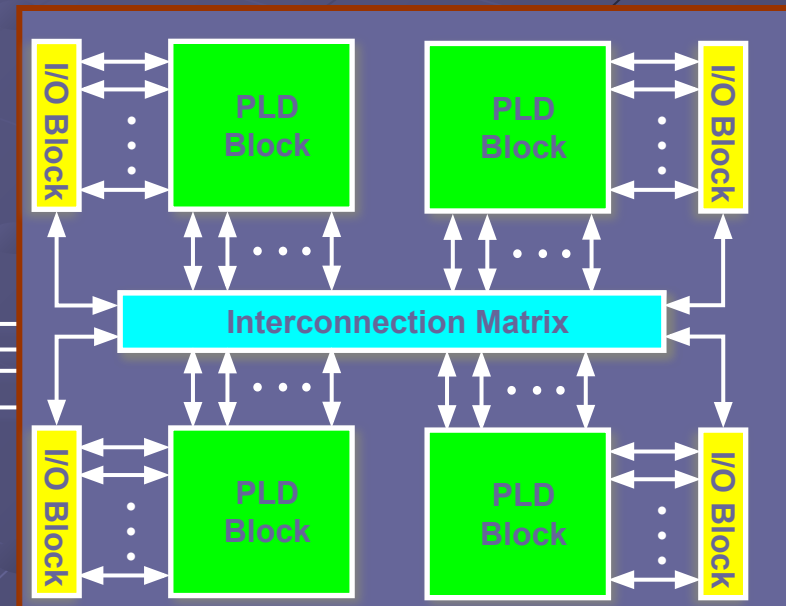
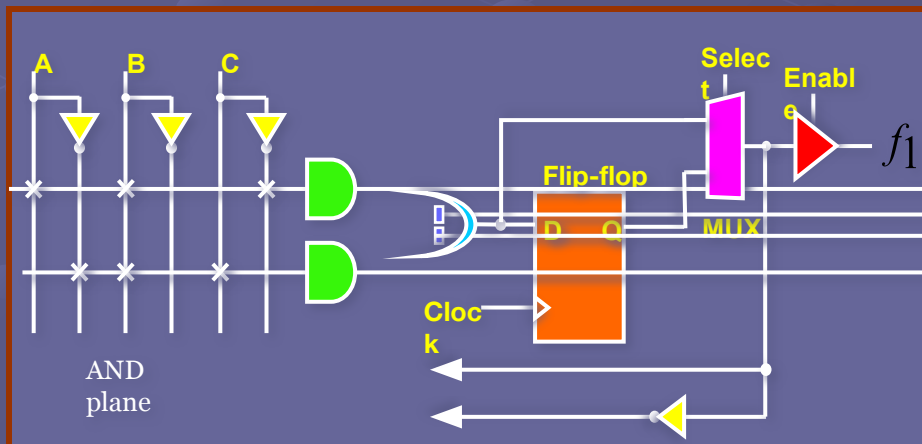
How it Began : PLA

- Programmable Logic Array
- First programmable device
- 2-level and-or structure
- One time programmable



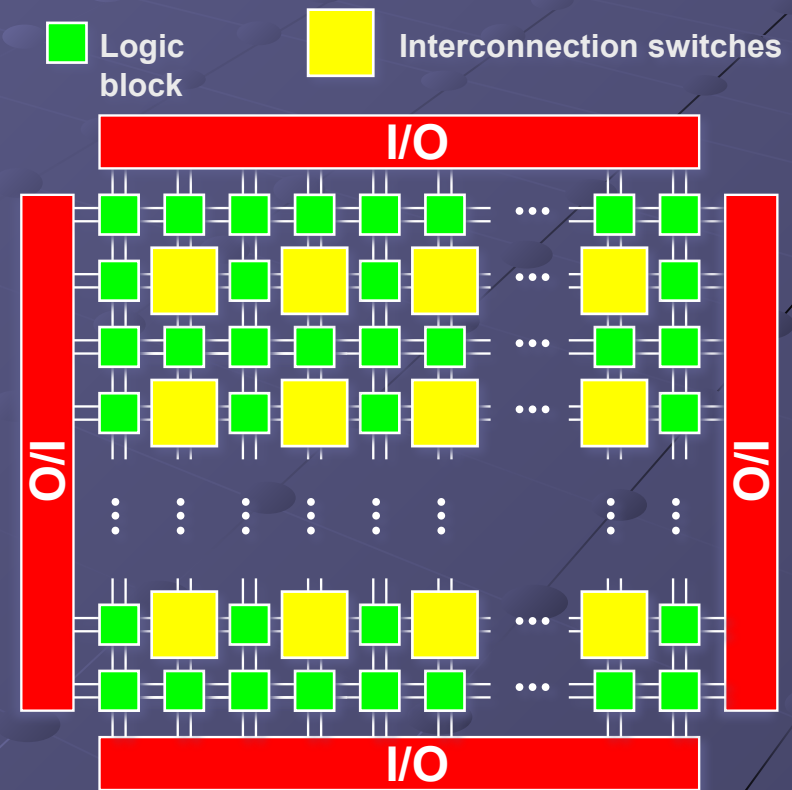
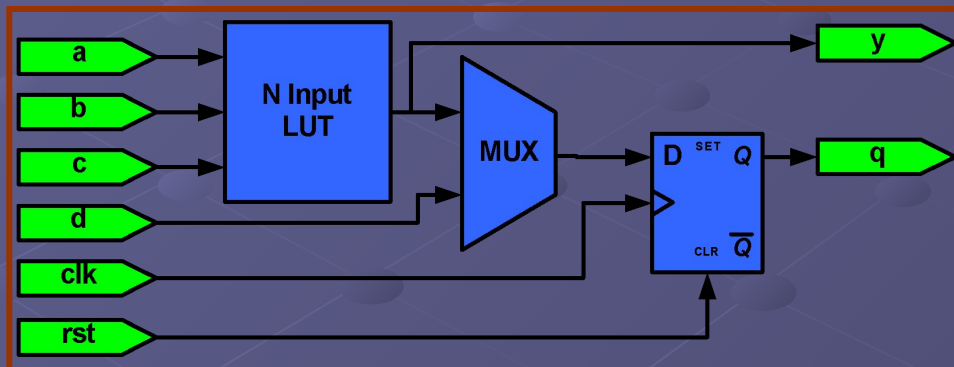
SPLD - CPLD

- Simple Programmable logic device
 - Single AND Level
 - Flip-Flops and feedbacks
- Complex Programmable logic device
 - Several PLDs Stacked together



FPGA - Field Programmable Gate Array

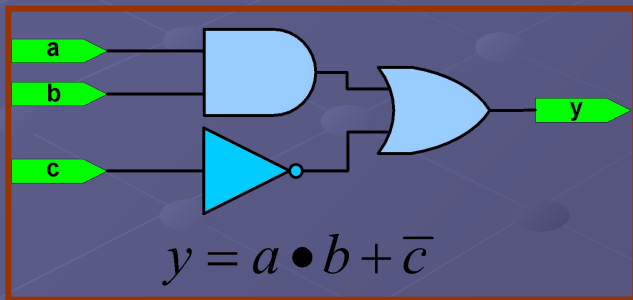
- Programmable logic blocks (Logic Element “LE”)
Implement combinatorial and sequential logic. Based on LUT and DFF.
- Programmable I/O blocks
Configurable I/Os for external connections supports various voltages and tri-states.
- Programmable interconnect
Wires to connect inputs , outputs and logic blocks.
 - clocks
 - short distance local connections
 - long distance connections across chip



Configuring LUT

- LUT is a RAM with data width of 1bit.
- The contents are programmed at power up

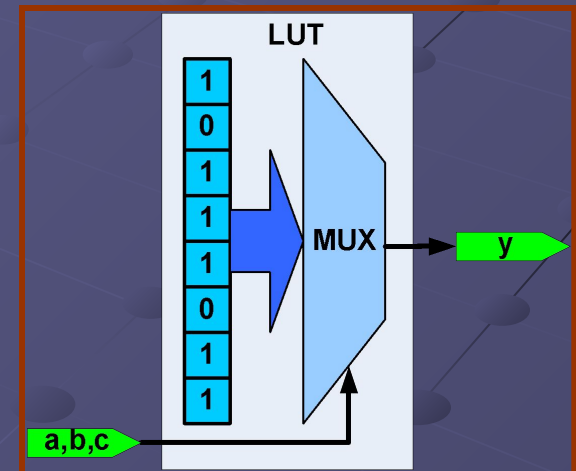
Required Function



Truth Table

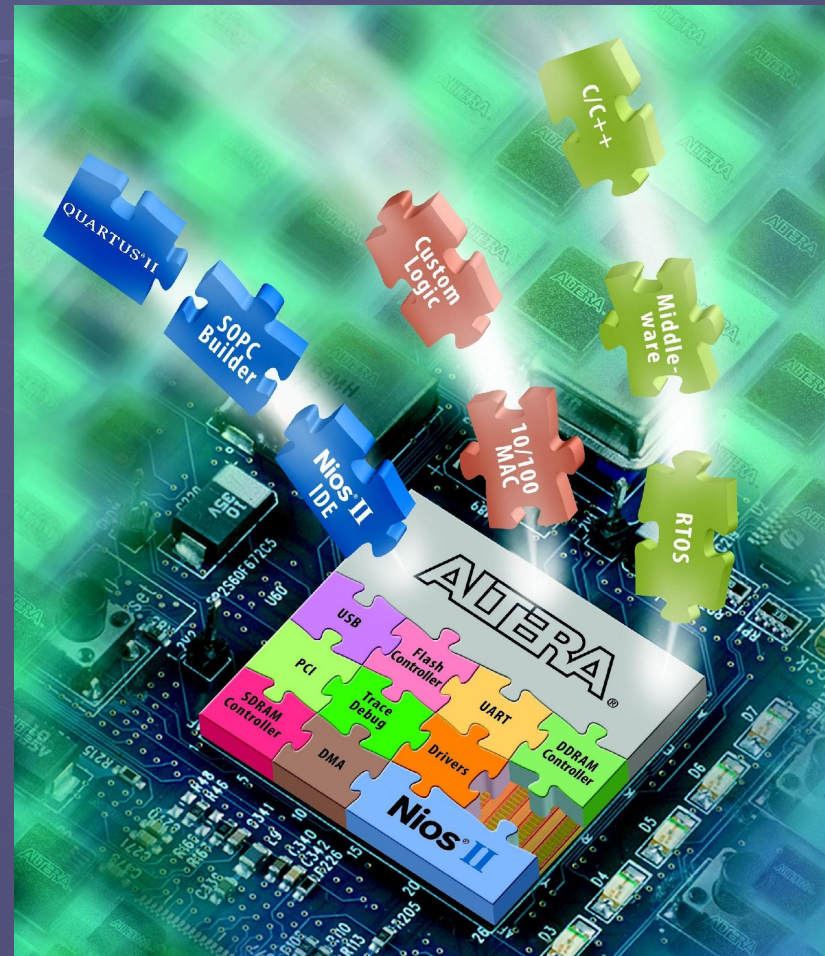
a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Programmed LUT

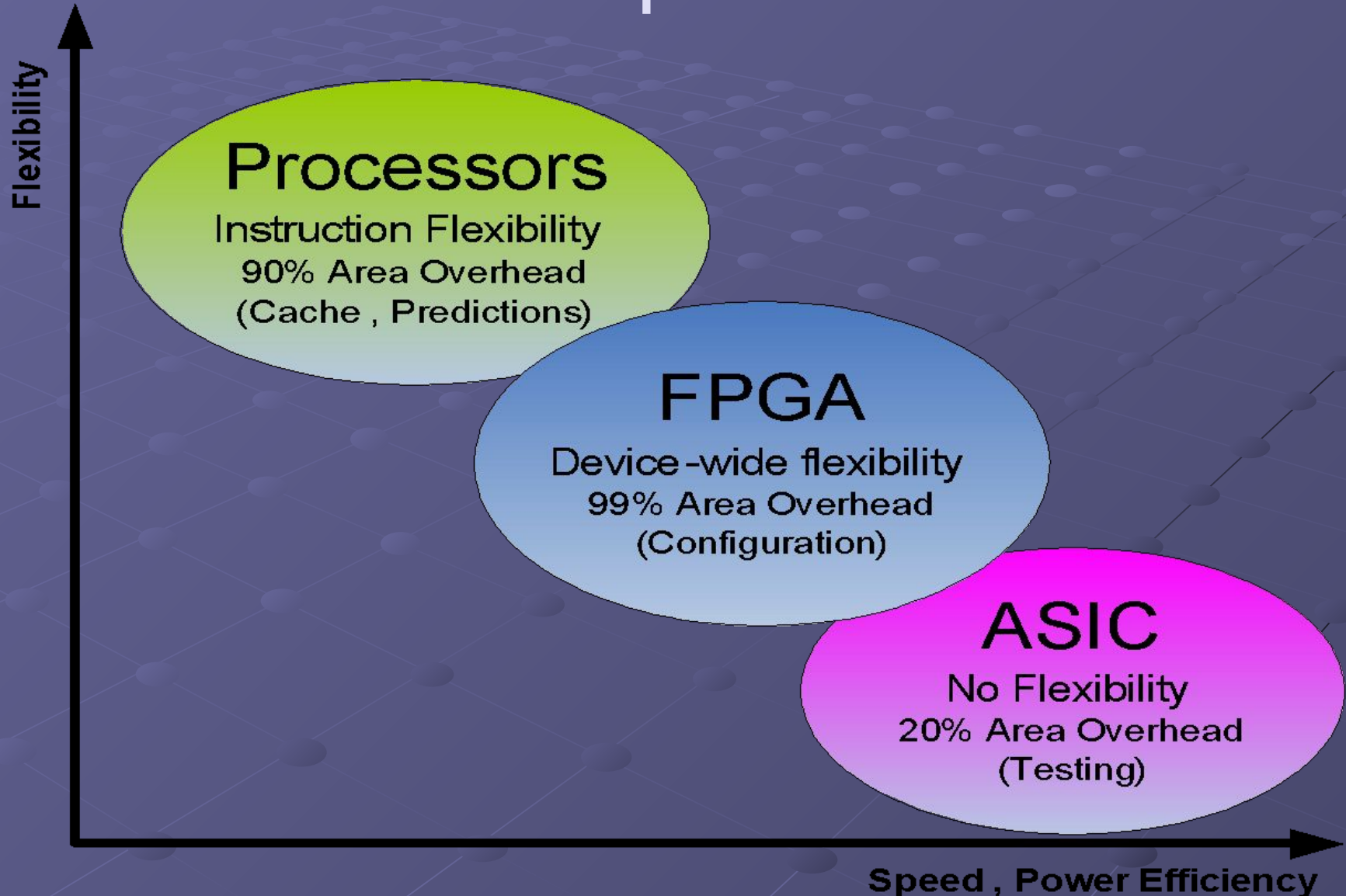


Special FPGA functions

- Internal SRAM
- Embedded Multipliers and DSP blocks
- Embedded logic analyzer
- Embedded CPUs
- High speed I/O (~10GHz)
- DDR/DDRII/DDRIII SDRAM interfaces
- PLLs



Comparison



Processors

Instruction Flexibility
90% Area Overhead
(Cache, Predictions)

FPGA

Device-wide flexibility
99% Area Overhead
(Configuration)

ASIC

No Flexibility
20% Area Overhead
(Testing)

Speed, Power Efficiency

Usages

- Digital designs where ASIC is not commercial
- Reconfigurable systems
- Upgradeable systems
- ASIC prototyping and emulation
- Education

Manufacturers

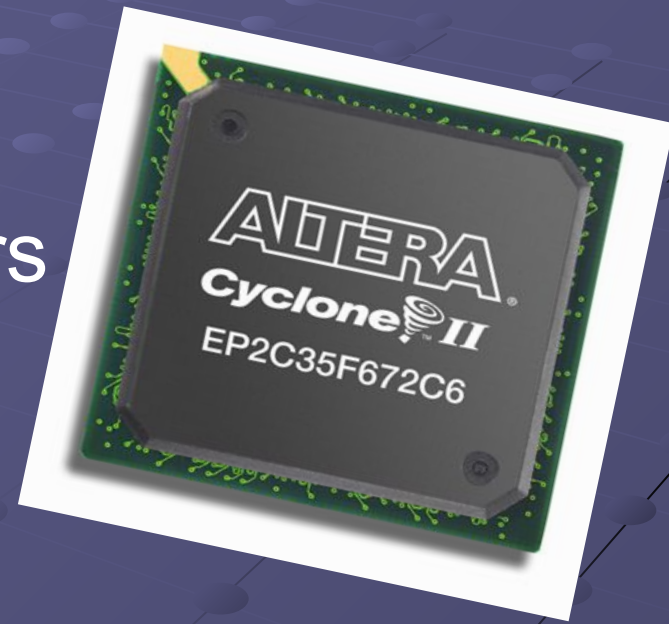
- Xilinx
- Altera
- Lattice
- Actel



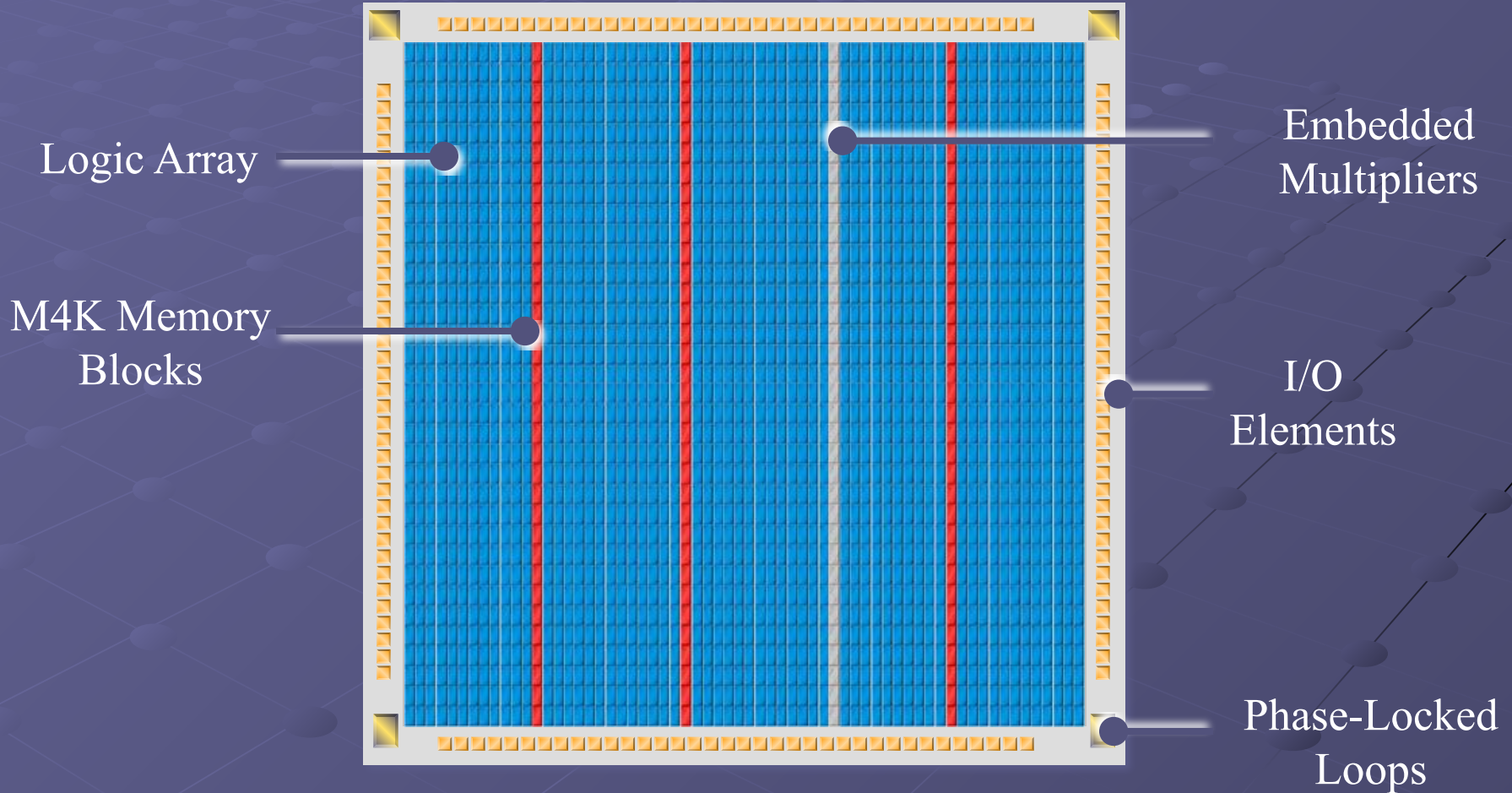
We will work with Altera FPGAs

Cyclone II - 20

- 18,752 LEs
- 52 M4K RAM blocks
- 240K total RAM bits
- 52 9x9 embedded multipliers
- 4 PLLs
- 16 Clock networks
- 315 user I/O pins
- SRAM Based volatile configuration

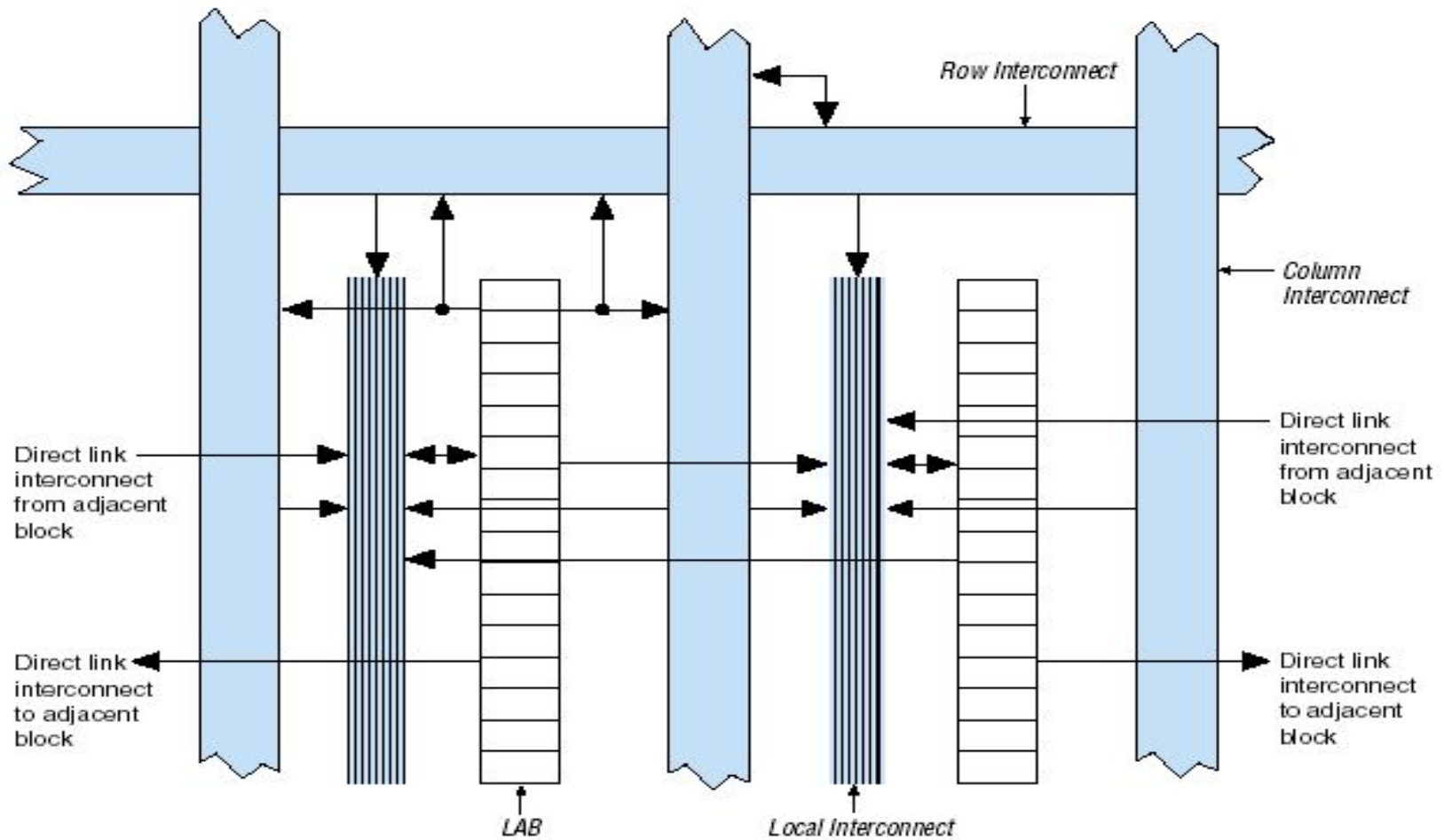


Cyclone II Internals



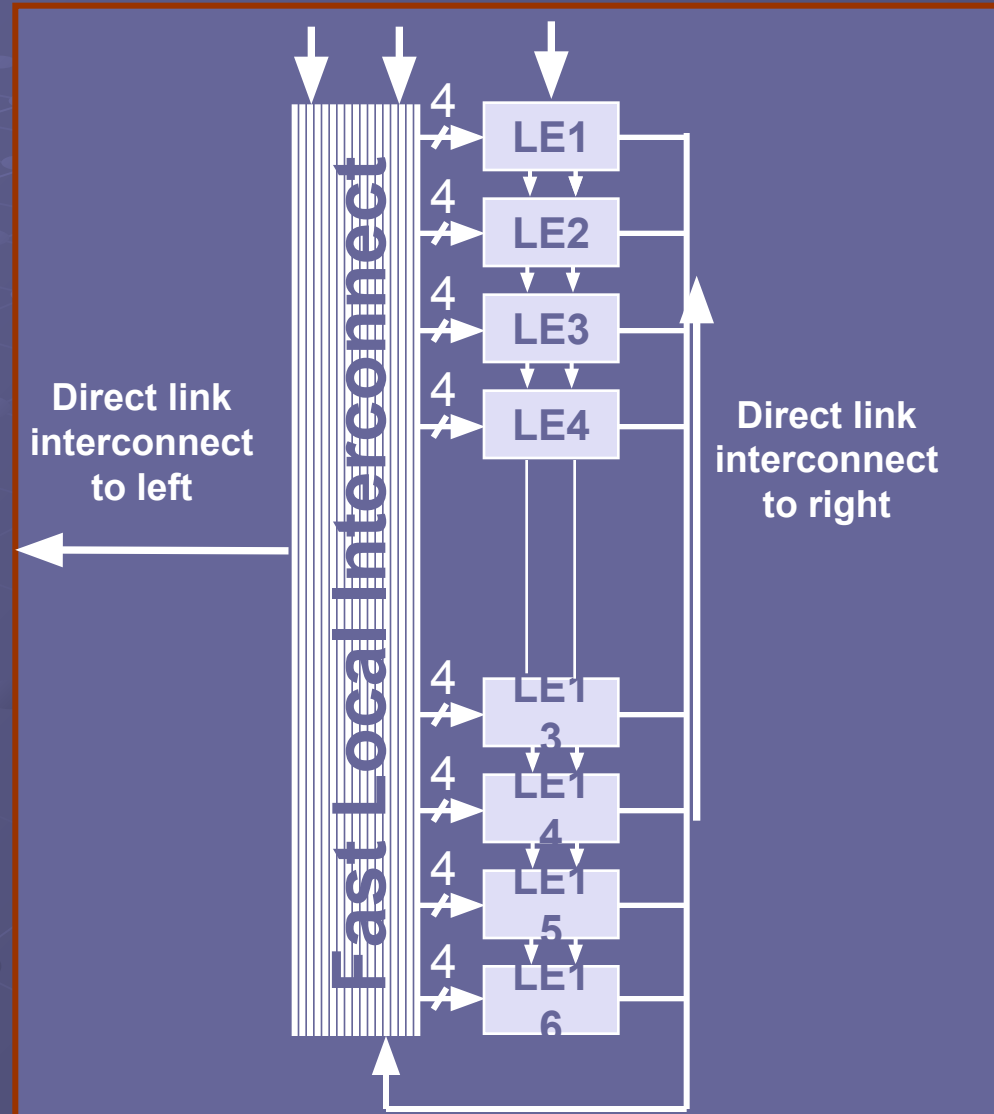
Cyclone II Logic Array

- Build of LABs (logic array blocks) and reconfigurable interconnect

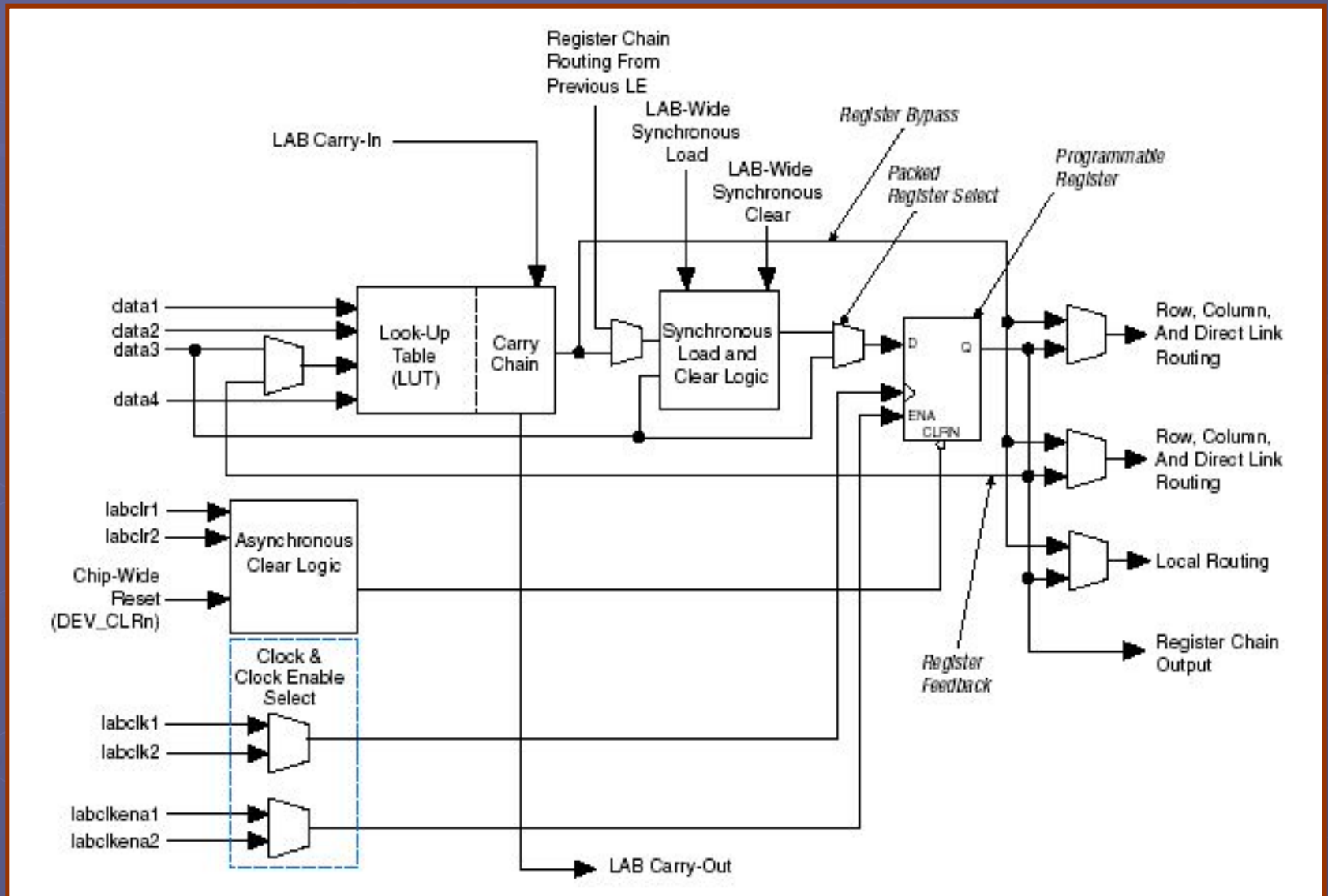


Cyclone II Logic Array Block (LAB)

- 16 LEs
- Local Interconnect
- LE carry chains
- Register chains
- LAB Control Signals
 - 2 CLK
 - 2 CLK ENA
 - 2 ACLR
 - 1 SCLR
 - 1 SLOAD

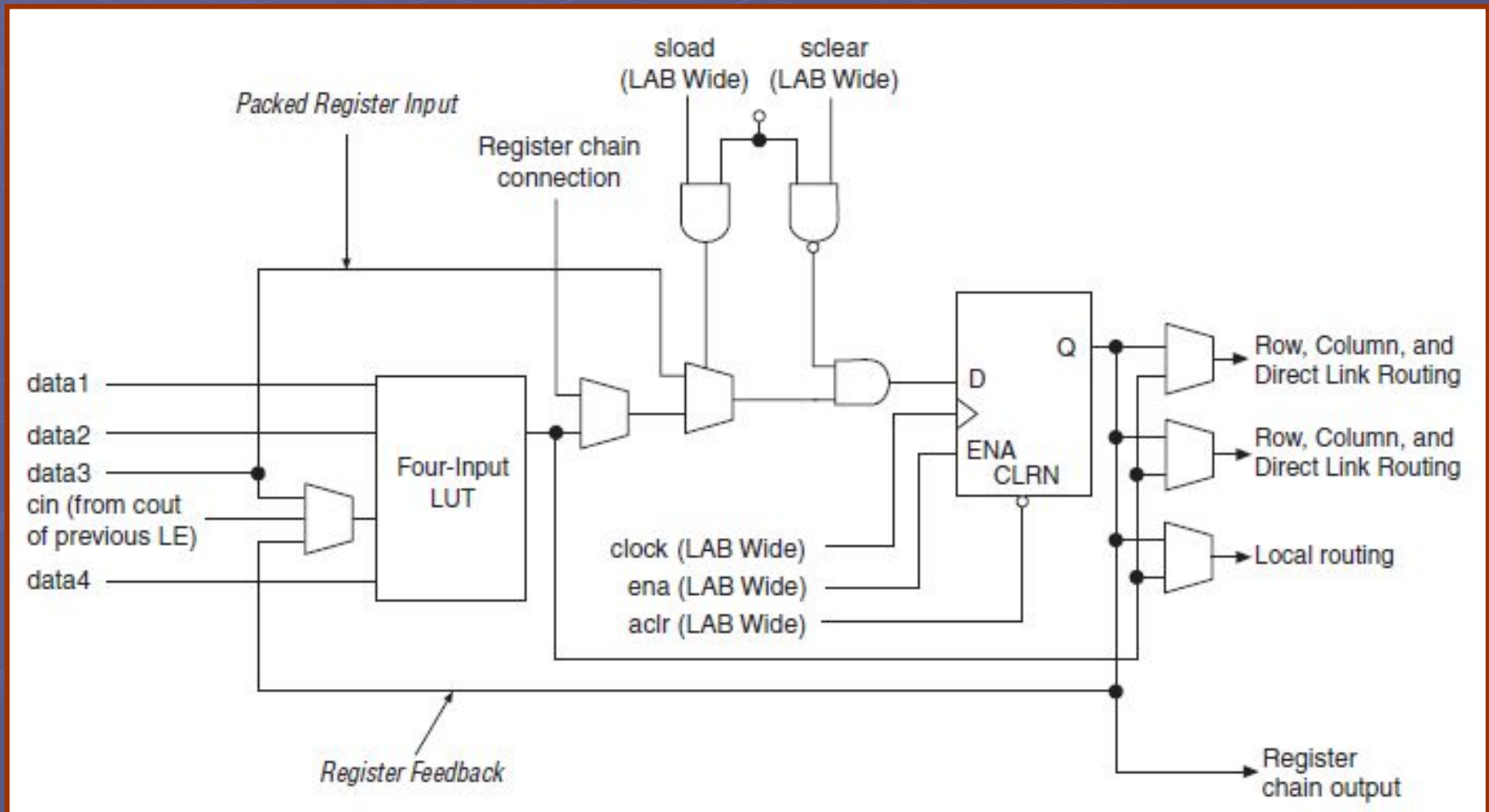


Cyclone II Logic Element (LE)



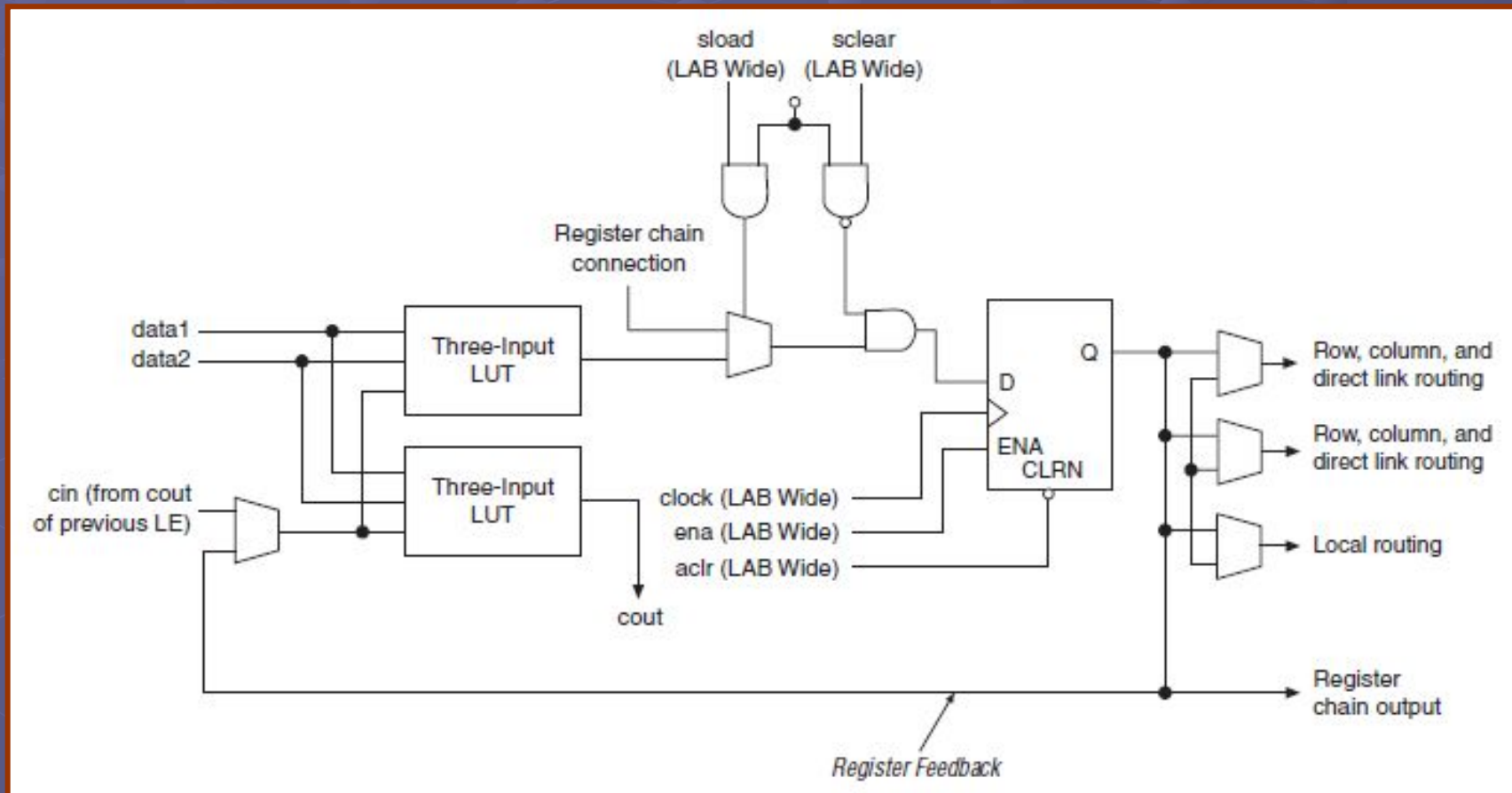
LE in Normal Mode

- Suitable for general logic applications and combinational functions.



LE in Arithmetic Mode

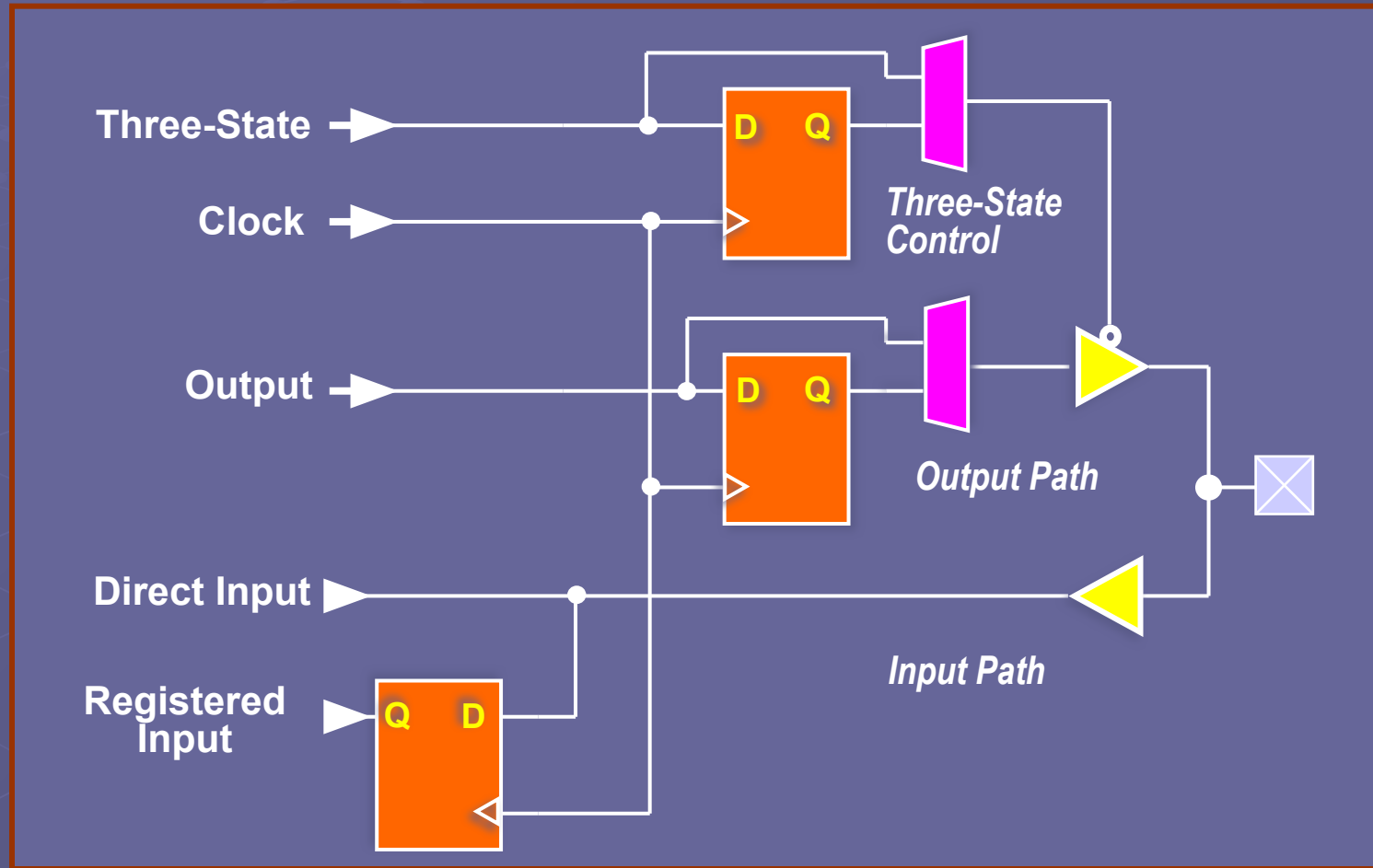
- Ideal for implementing adders, counters, accumulators, and comparators.



Cyclone II I/O Features

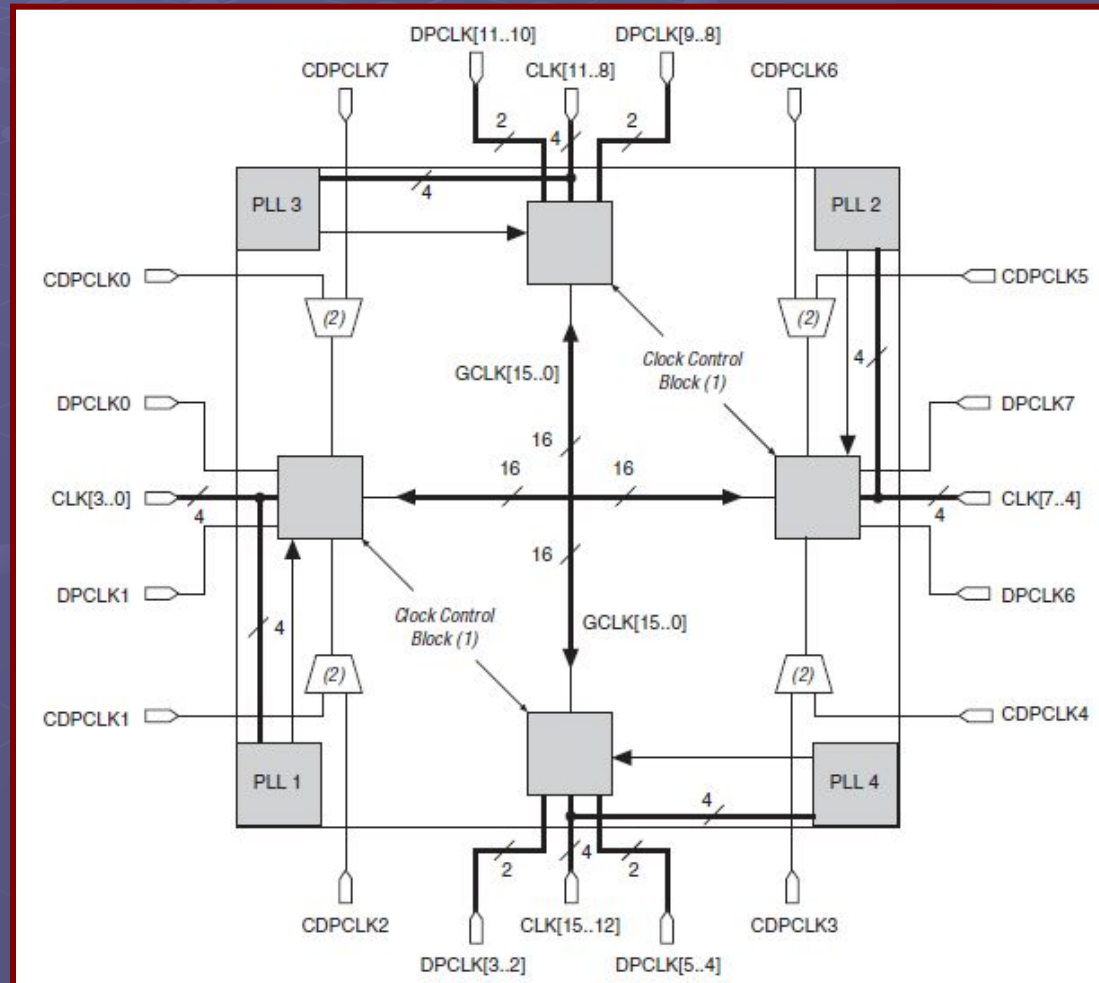
- In/Out/Tri-state
- Different Voltages and I/O Standards
- Flip-flop option
- Pull-up resistors
- DDR interface
- Series resistors
- Bus keeper
- Drive strength control
- Slew rate control
- Single ended/differential

Cyclone II I/O Buffer



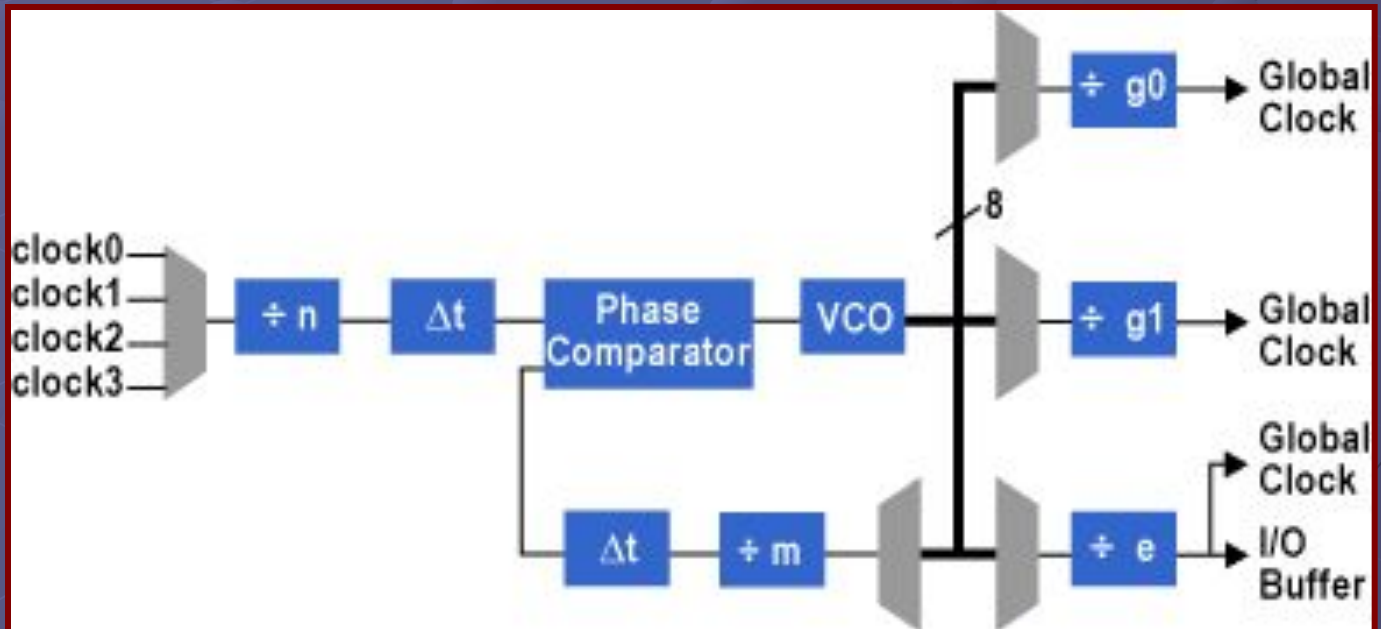
Cyclone II Clocking

- 16 Global Clocks
- 4 PLLs



Cyclone II PLL

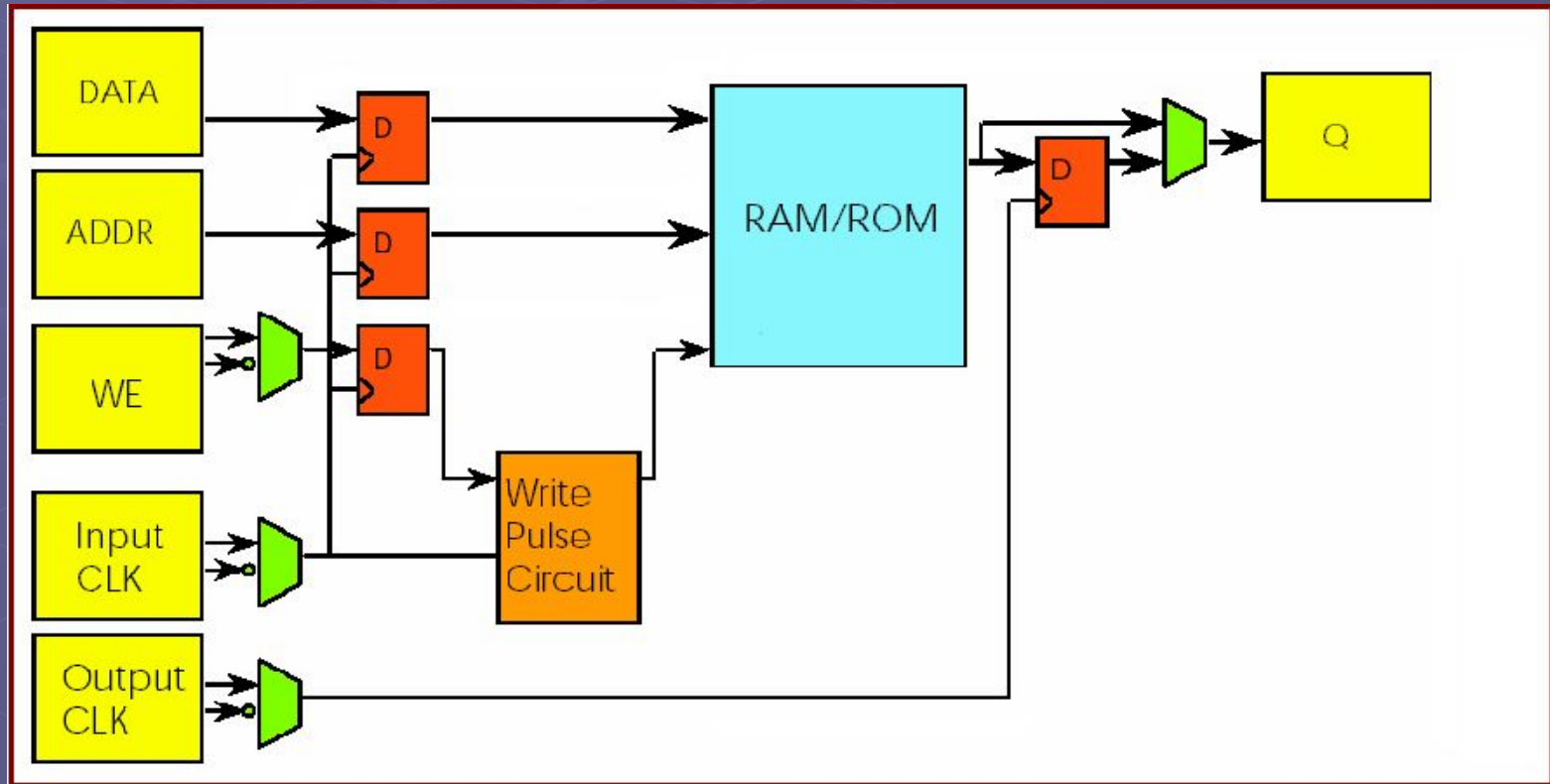
- 3 Outputs
- Clock Division
- Clock Multiplication
- Phase shift



Memory

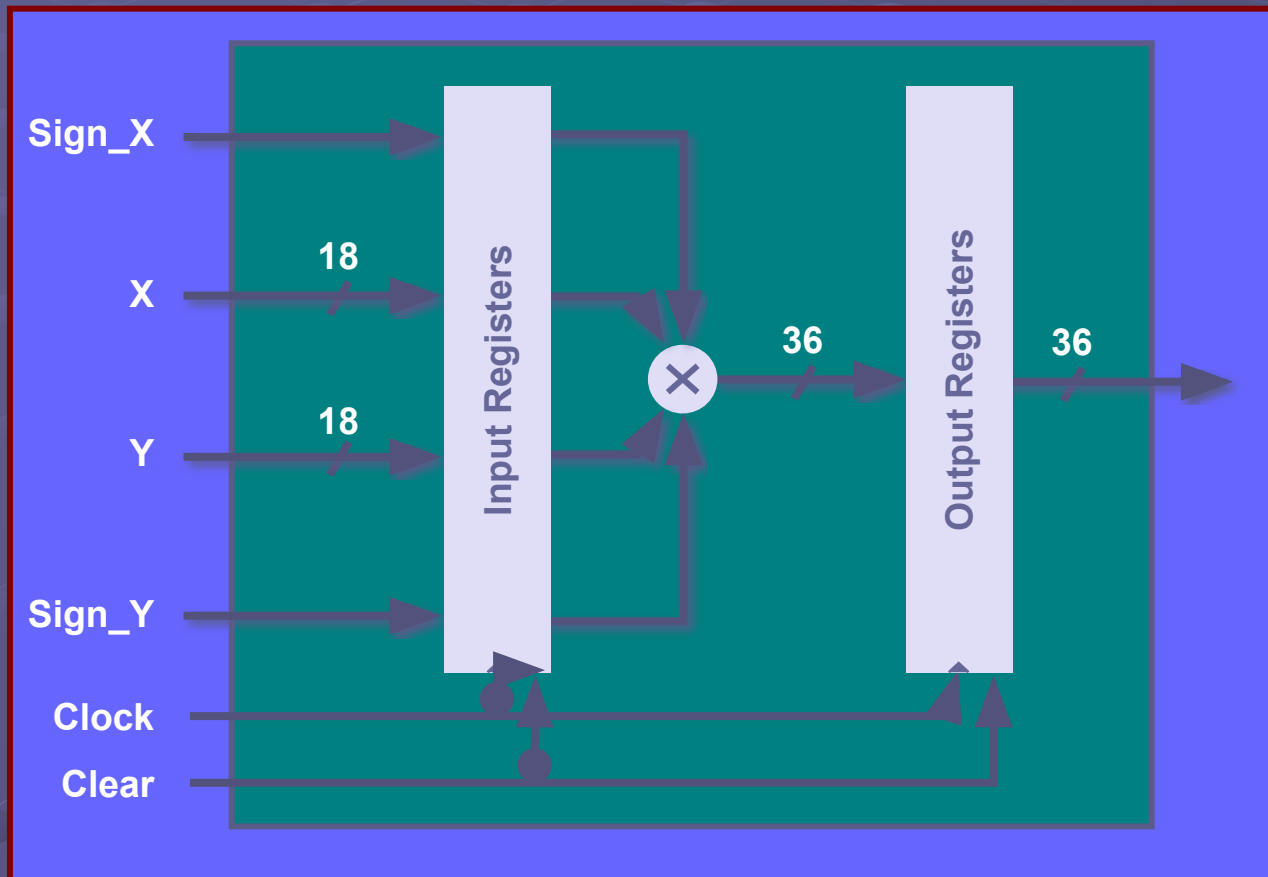
- True Dual port RAM/ROM with dual clock
- Variable data width
 - 4K×1, 2K×2, 1K×4, 512×8, 512×9, 256×16, 256×18
 - 128×32, 128×36 (not available in true dual-port mode)
- Input data and address are registered
 - 1 Clock Write latency
- Output data can be registered
 - Read latency of 1 or 2 clocks
- Byte Enable

Cyclone II Memory Structure



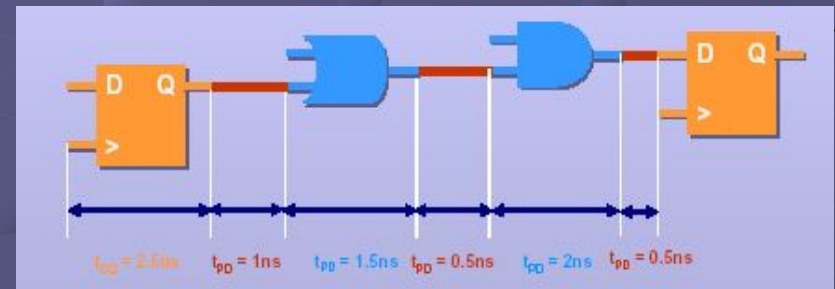
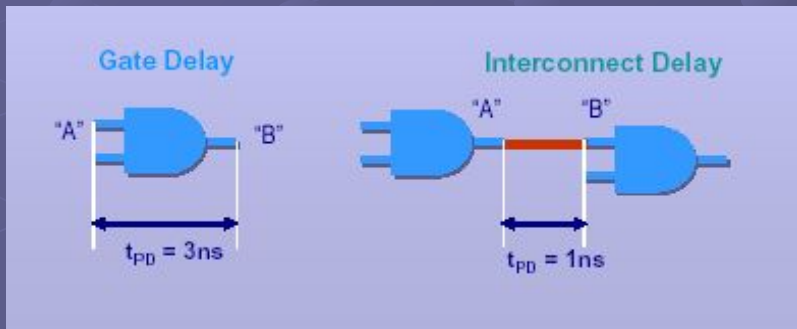
Cyclone II Multipliers

- 18x18 or 2 9x9 modes
- Up to 250MHz Performance



Delays and maximal frequency

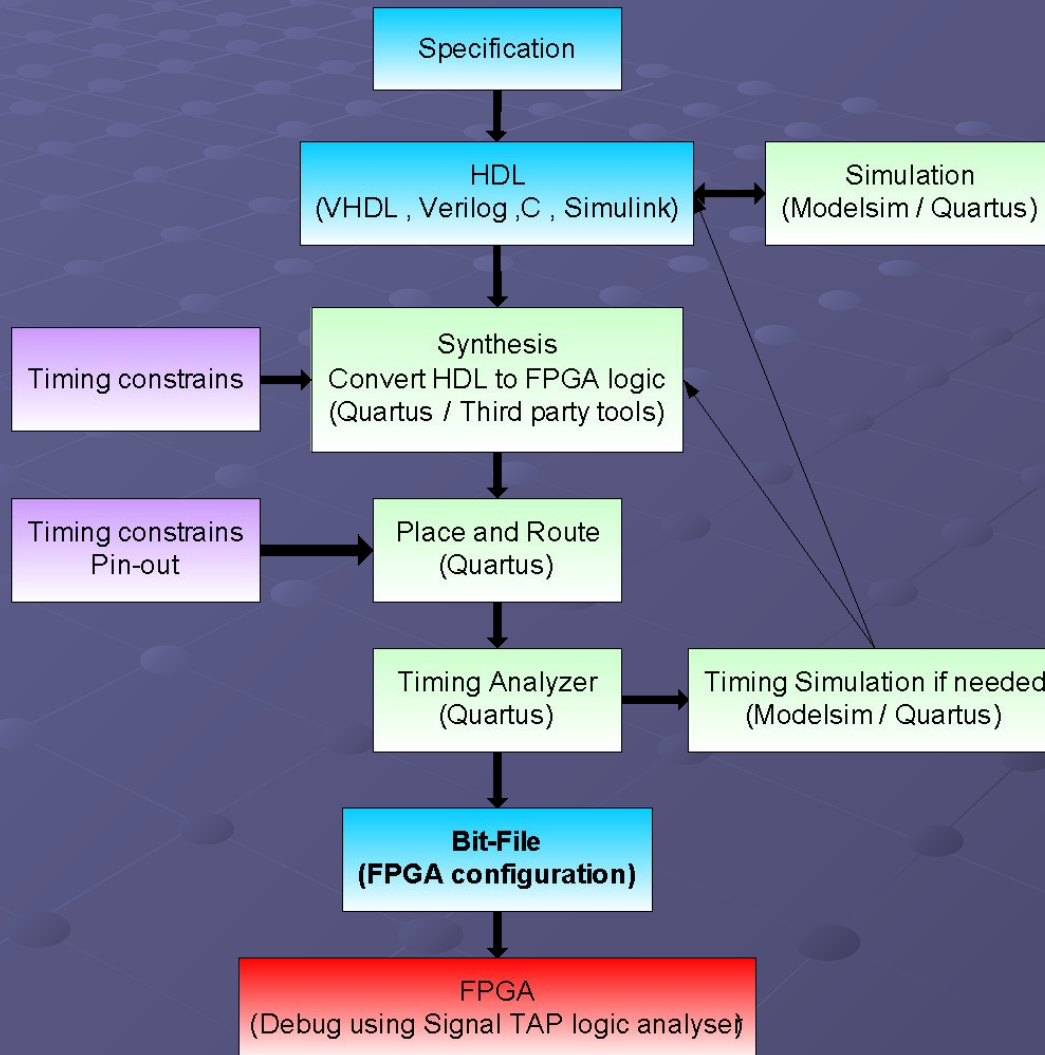
- Gate delay – Delay of logic element
- DFF delay t_{co} (t_{su} - Very small)
- Interconnect delay



$$1/F_{\max} = T_{co} + T_{pd}_{\text{logic}} + T_{pd}_{\text{interconnect}}$$

Maximum Frequency is the fastest speed a circuit containing flip-flops can operate.

Design flow



Design Rules

	ASIC	FPGA
Adder	CLA	Ripple Carry
Latch	Commonly used	Not Recommended
Gated clock	Commonly used	Unacceptable
Tri-State	Commonly used	Only in I/O
Async RAM	Commonly used	Only Small



Any questions?