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动作原理浅谈之
S3(Standby)/S4(Hibernate)

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Agenda

- What is S3/S4? And what's the benefit?
- S3/S4 power system and control sequence?
- How to implement S3/S4??
- How to debug S3??

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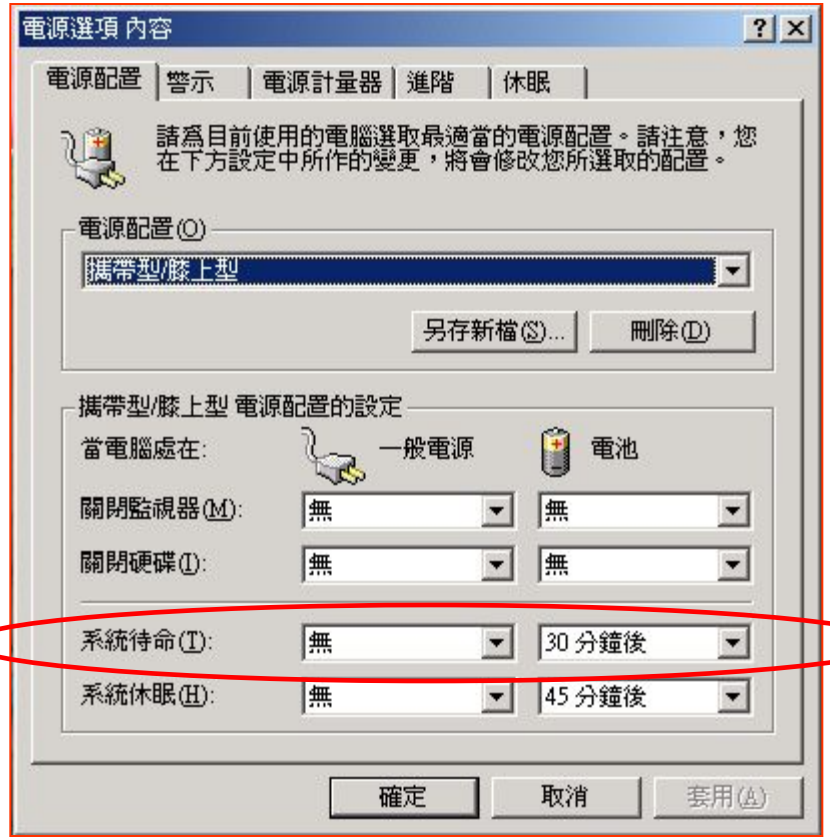
What is S3/S4 ??

S3,S4在ACPI的定义:

S3—Suspend to Ram (STR): The system context is maintained in system DRAM, but power is shut off to no-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.



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What is S3/S4 ??

S3,S4在ACPI的定义:

S4—Suspend to Disk (STD):

The system context is maintained on the disk. All power is then shut off to the system except for the logic required to resume.

ACPI:
1996 年时，由微软(Microsoft)、英特尔(Intel)与东芝(Toshiba)主导，共同制定了业界以「操作系统」为标准的电源管理程序ACPI(Advanced Configuration & Power Interface)，正式把电源管理工作交给操作系统来负责.

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ACPI Power Management Spec.

S1 Sleeping State

The S1 sleeping state is a low wake latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

S2 Sleeping State

The S2 sleeping state is a low wake latency sleeping state. This state is similar to the S1 sleeping state except that the CPU and system cache context is lost (the OS is responsible for maintaining the caches and CPU context). Control starts from the processor's reset vector after the wake event.

S3 Sleeping State

The S3 sleeping state is a low wake latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake event.

S4 Sleeping State

The S4 sleeping state is the lowest power, longest wake latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is maintained.

S5 Soft Off State

The S5 state is similar to the S4 state except that the OS does not save any context. The system is in the "soft" off state and requires a complete boot when it wakes. Software uses a different state value to distinguish between the S5 state and the S4 state to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

ACPI定义了以下几种状态规范：

ACPI 电源管理标准把操作系统、硬件环境、省电作用等，分成五种状态做规划，分别是G（Global）系统状态、D（Device）装置状态、S（Sleeping）休眠状态，C（CPU）处理器状态以及P（Performance）state.

- 1. Global System State Definitions---G state
- 2. Device Power State Definitions---D state
- 3. Sleeping State Definitions---S state
- 4. Processor Power State Definitions---C state
- 5. Device and Processor Performance State Definition---P state

What's the benefit of S3/S4??

- S3-STR(Suspend to RAM,休眠到内存)
- 優點:启动速度特别快,而且可以保留工作状态,同時此模式的耗电最少,速度也够快,达到最省电和无噪音的效果.

- 缺點:因數據保存于內存,系統不能完全斷電且很容易因为第三方驱动程序的兼容性问题使得系统无法正常进入Suspend状态.同時BIOS对ACPI的支持不完善,也会使STR功能无法使用。

- S4-STD(Suspend to Disk,休眠到硬盘)
- 優點:启动速度較系統開機快且可以保留工作状态,同時此模式不耗電,速度也較快, 在系統完全掉電後不會丢失任何信息.

- 缺點:數據保存于HDD,在進入休眠狀態時需要保存桌面及所有打開文件和文檔的映像至HDD,相比S3待機速度較慢.

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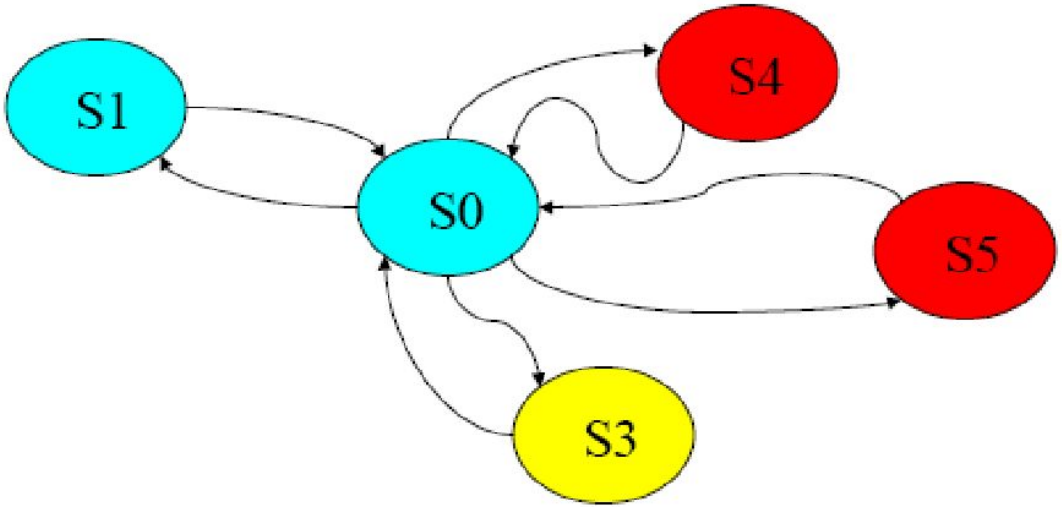
S3/S4 Power system and control sequence

Power Name & System State Table

System State / Power Name	S0	S1	S3	S4	S5
XXV_S0	ON	ON	OFF	OFF	OFF
XXV_S3	ON	ON	ON	OFF	OFF
XXV_S5	ON	ON	ON	ON	ON



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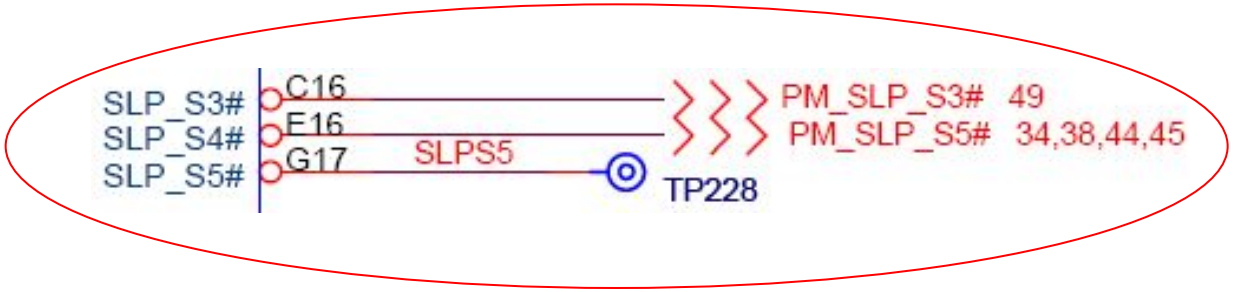
Control Signals

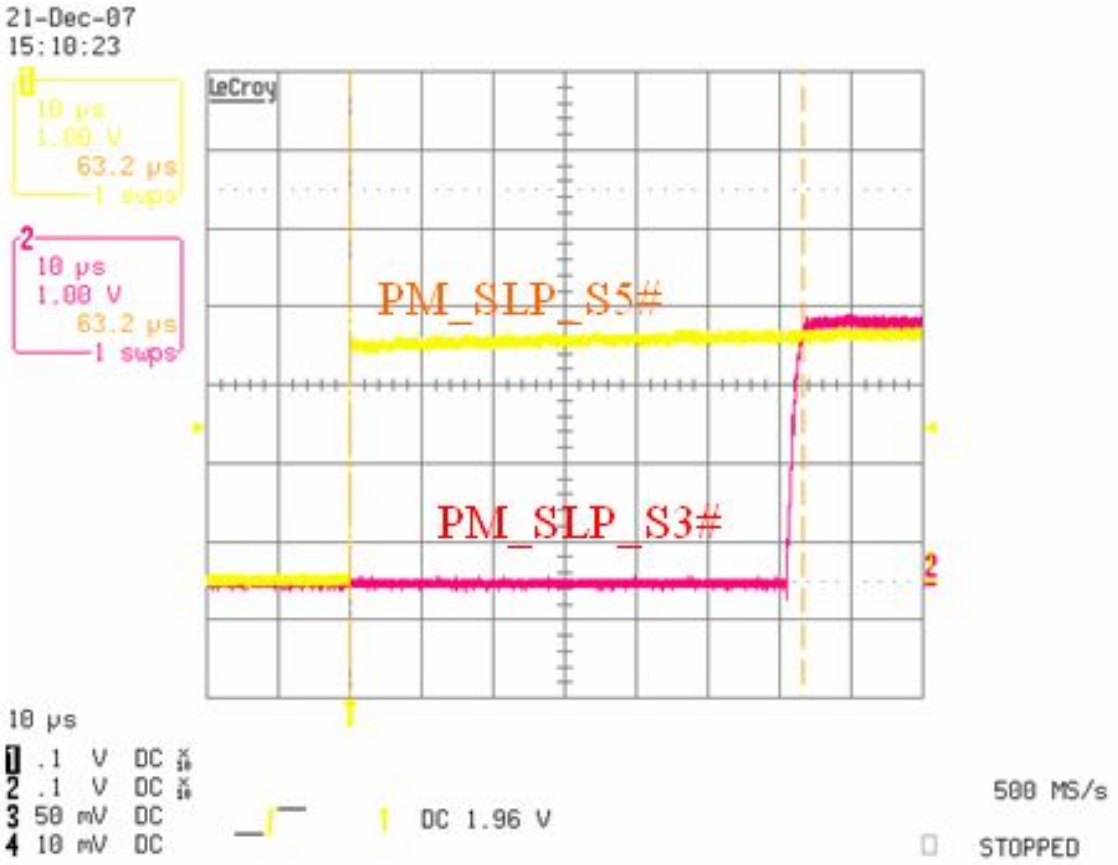
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control**: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power in order to use the ICH9's DRAM power-cycling feature. Refer to Chapter 5.13.11.2 for details. **NOTE:** In a system with Intel AMT or ASF support, this signal should be used to control the DRAM power. In M1 state (where the host platform is in S3–S5 states and the manageability sub-system is running) the signal is forced high along with SLP_M# in order to properly maintain power to the DIMM used for manageability sub-system.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.



Power on sequence

T234	Min	Max	Measure
	1RTCCLK		63.2us

1RTC CLK is approximately from 28.992us to 32.044us.



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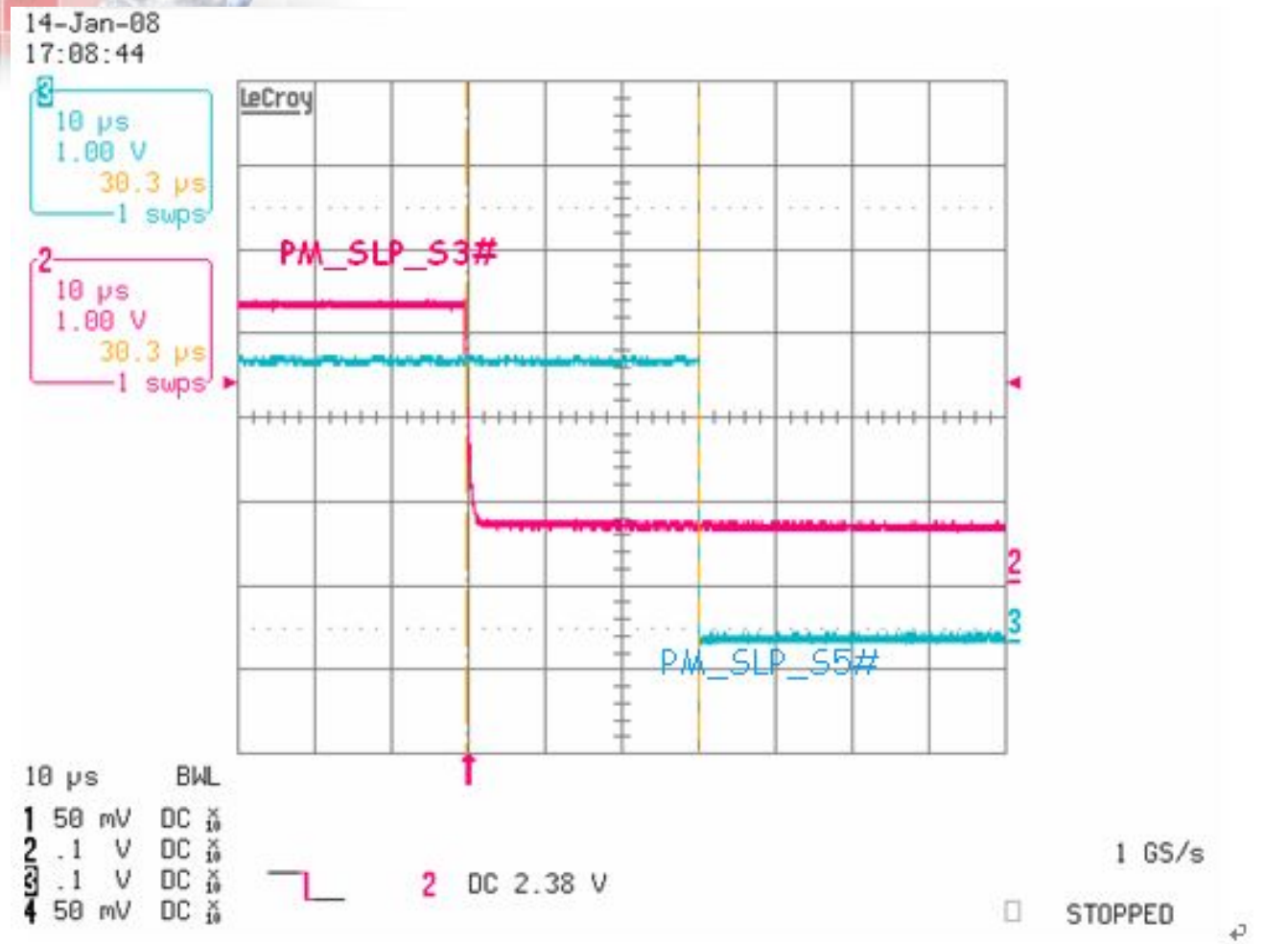
Power off sequence



t291	SLP_S3# active to SLP_S4# active	1	2	RTCCLK	1

SPEC=30us < T=30.3us <SPEC=60us can meets SPEC

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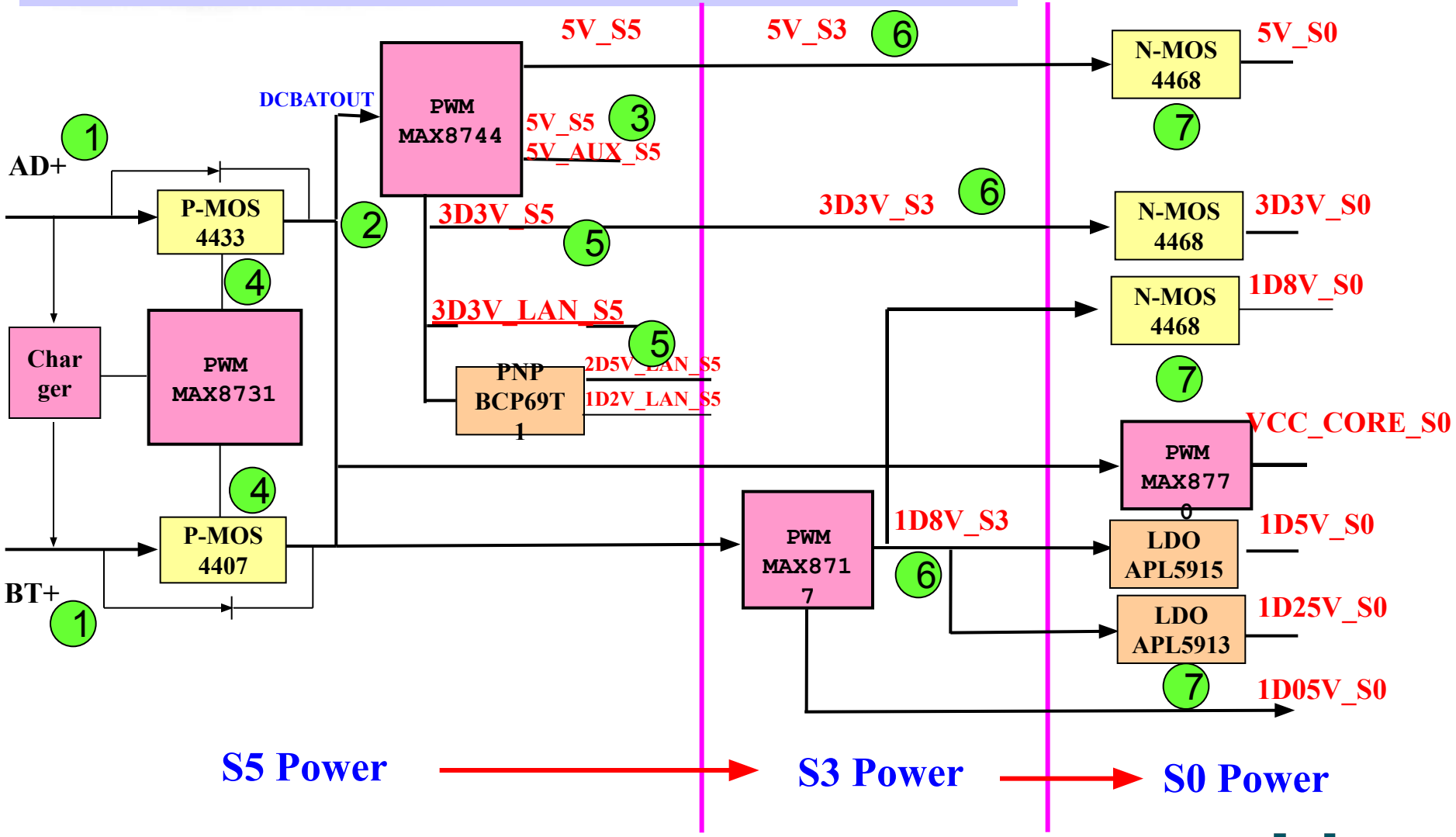
Power system architecture

1 Tahoe power system architecture :



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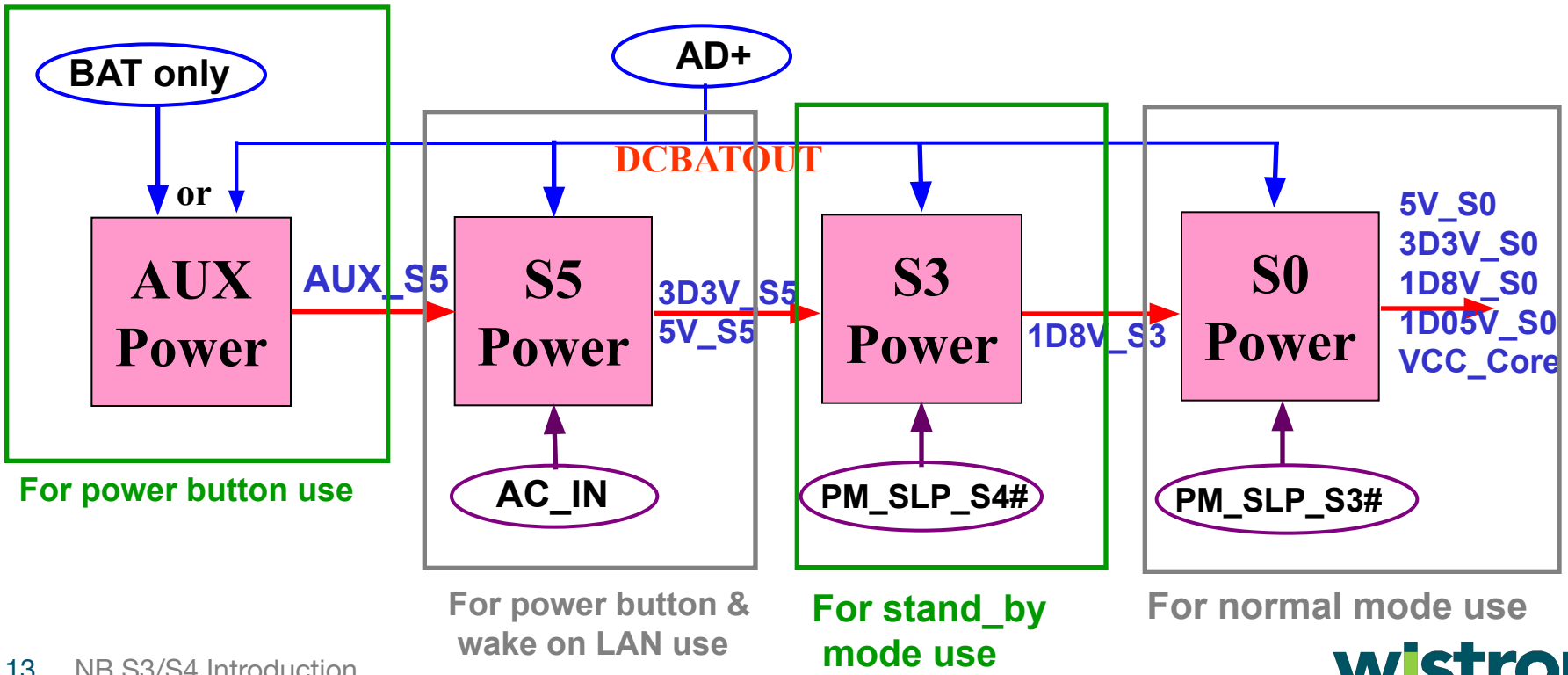
Power system architecture

3 Power sequence and control :

Q1. Why we need to separate the powers to AUX,S5,S3,S0 ?

Q2. How to control them ?

The answer showed as below :



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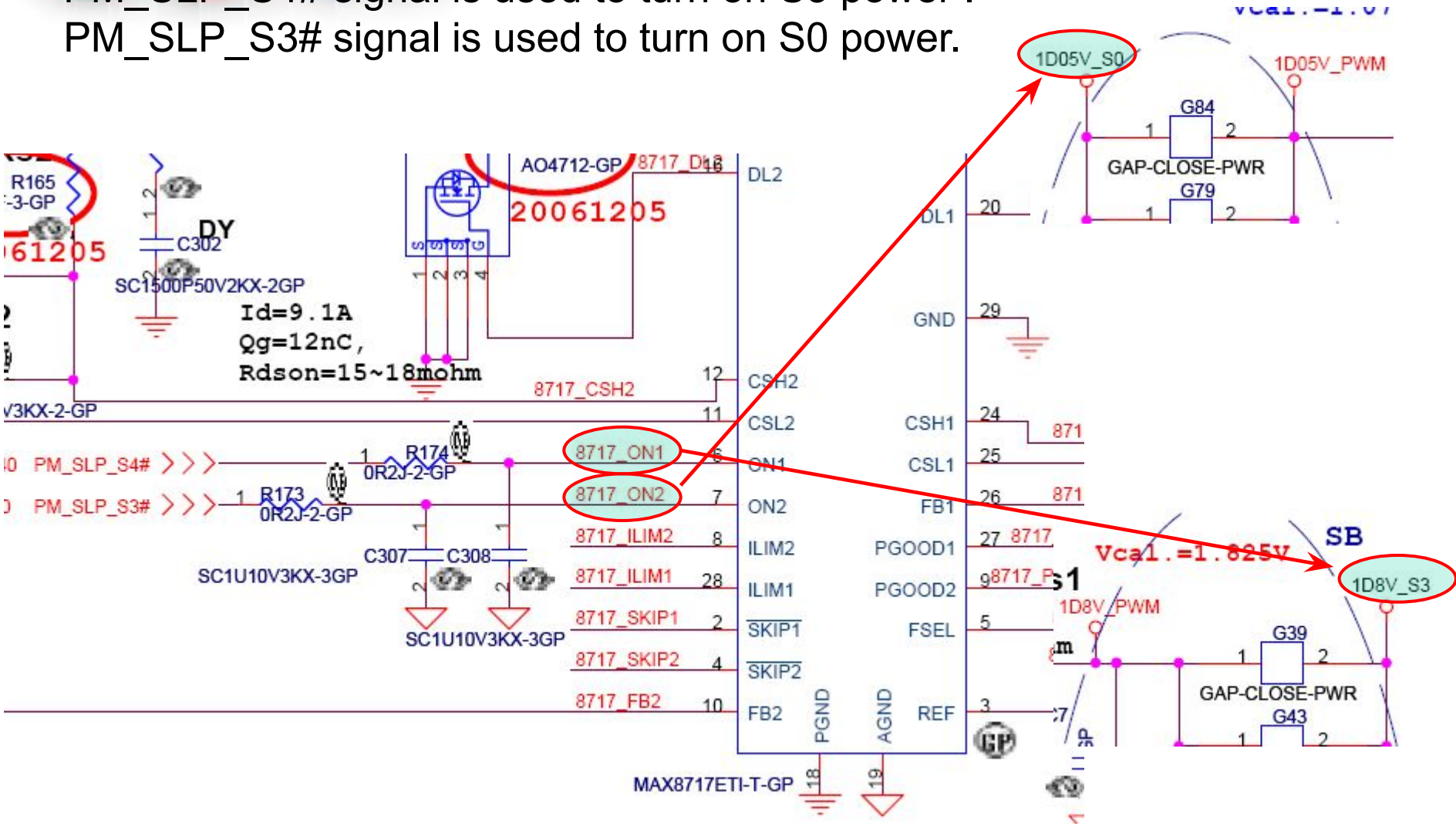
Power sequence

PM_SLP_S4# signal is used to turn on S3 power .
PM_SLP_S3# signal is used to turn on S0 power.



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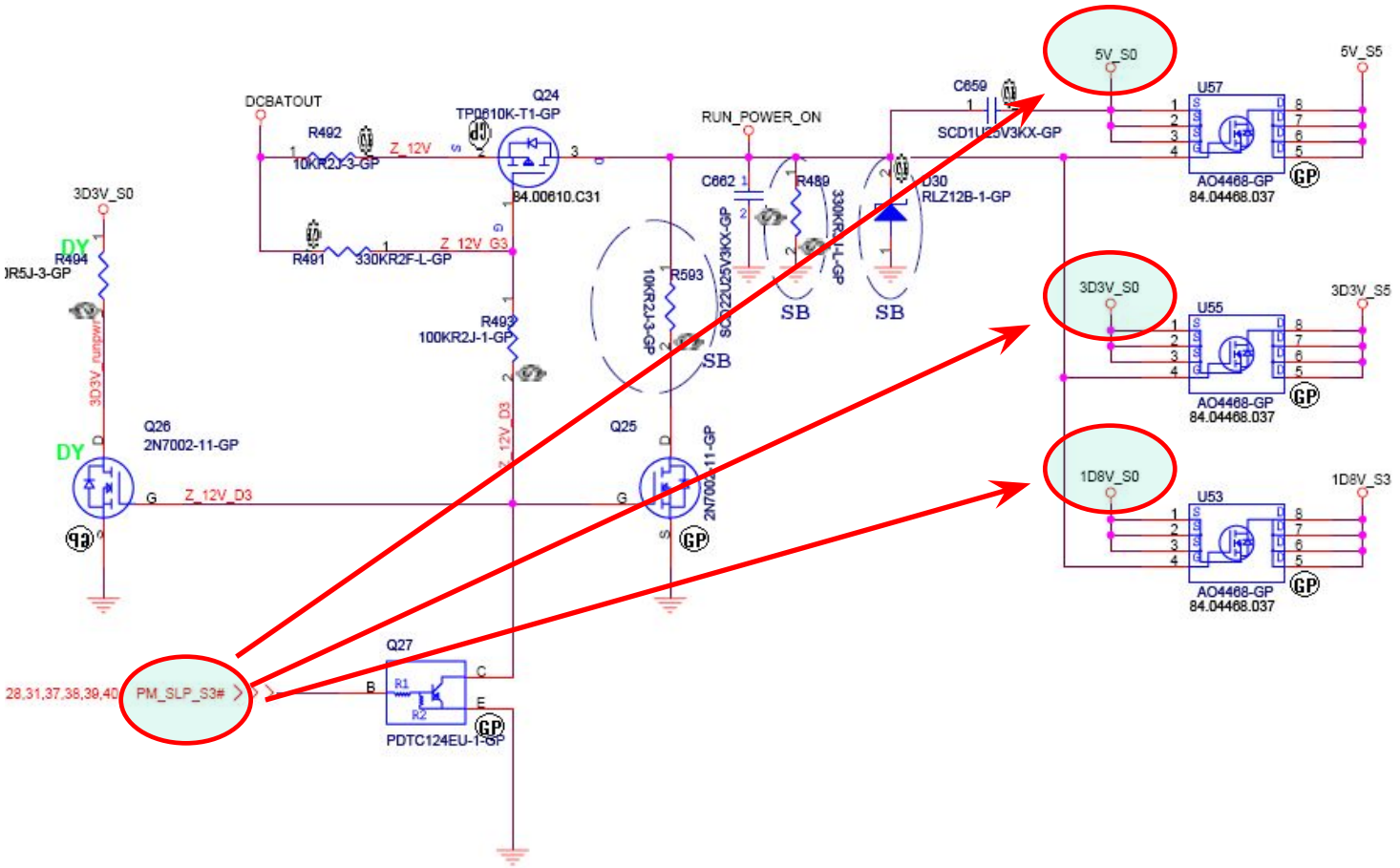
Power sequence

Circuit operation S0 power :

PM_SLP_S3# signal is used to turn on 5V、3D3V、1D8V_S0 also .



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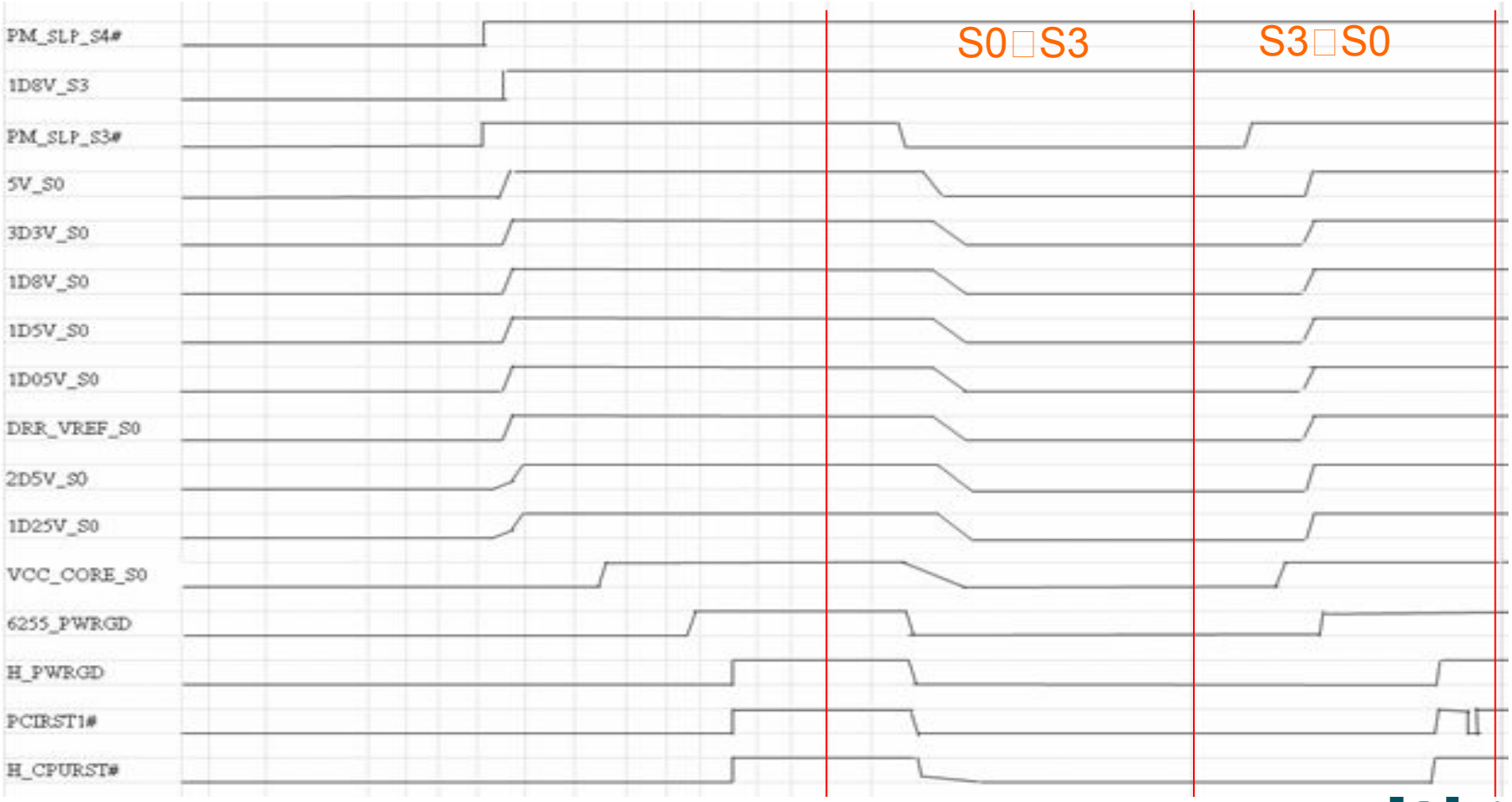
Stand-by动作原理

- S3 Entry process:
- When user issue S3 event (Fn+Fx ,power button, LID switch), BIOS will issue to OS,then OS will notice all driver to execute S3 process. After OS finish standby process . BIOS will enable SWI. Then BIOS notice chipset to turn off S0 power.(keep S3 power alive).
- S3 Resume process:
- When Wake Event be issued, KBC will issue SWI to south bridge or south bridge get PME# from PCI device or south bridge get PWRBT# from power button, then south bridge will issue SLP_S3# to turn on S0 power again. Then BIOS will restore OS data from DIMM, then back to OS working mode.

Standby動作原理

Standby(S0⇄S3)實現動作原理:

S3 ⇄S0 power sequence



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Hibernation動作原理

Standby(S0⇄S4)實現動作原理:

1. 當系統接到Hibernation指令後會將當前文檔,桌面,工作狀態等數據映像寫入HDD內並更改HDD引導區.
2. 所有數據都寫入HDD後系統會依照power off sequence將各reset power依此關掉進入完全關機狀態.
3. S4喚醒時完全follow power on sequence各power reset會依次打開,CPU正常運作後開始讀取HDD內邏輯引導區引導讀取映像文件,系統恢復到之前狀態.

Standby VS Hibernation

Contrast between Standby and Hibernation power

Standby VS Hibernation					
類型	休眠至	enable	S5	S3	S0
standby		PM_SLP_S3#	ON	ON	OFF
Hibernation (ADT)		PM_SLP_S4#	ON	OFF	OFF
Hibernation (BAT)		PM_SLP_S4# S5_Enable	OFF	OFF	OFF

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How to implement S3??

- Check SW whether support ACPI spec.
- Check MRS(Marketing Requirement Spec.) support what kind of S3 wake event.
- -Power button,LID,BL2
- -USB, WOR,WOL, Any-key wake
- -LAN, Card-Bus,IEEE 1394 (PCI PME#)
- Check VGA support $D3_{hot}$ or $D3_{cold}$
- Check South Bridge Wake Up Interface
- Check KBC Wake Up interface
- Check Logic Gate design

How to implement S3??

- Wake Event Design:
- USB: If your system support USB S3 wake,you must provide 5V_S3 for USB power. And BIOS need to enable USB interface S3 wake event.
- WOR: If your system support Wake on Ring. You must support S3 power for pin17 of MDC connector. And Vendor's driver need to support wake up function.
- PCI Device Wake(LAN, Card-Bus, 1394): If your system support PCI device wake event, you must provide S3 power to AUX power pin of device. And connect PME# to south bridge's PME#.

How to implement S3??

- **Discrete VGA support D3hot or D3cold:**
- **D3cold:When system enter S3 state, all power of VGA will be turn off. But you need to check VGA driver can be supported or not.**
- **D3hot: When system enter S3 state, some graphic power is still alive. It means that S3 power leakage will be increased.**

- **South Bridge Wake Up Interface:**
- **1. Power Button(AUX power plane)**
- **2. SWI from KBC(S5 power plane)**
- **3. PME#, need pull high to S5 power plane or not(S3 or S5 power plane)**
- **4. AC_IN (S5 power plane)**
- **5. Other S5 power plane's GPIO, need to check their pull high power state.**

How to Debug S3??

- Step 1: check HW S0 power off sequence. And DIMM whether enter self-refresh mode normally.
- Step 2: check S5/S3 power is alive, and no leakage in S0 power(3D3V_S0,5V_S0,..)
- Step 3: check KBC or South bridge receive your wake signal.
- Step 4: check south bridge or KBC already send out power on signal.
- Step 5: check power on sequence. And DIMM's timing from self-refresh mode to normal refresh mode.
- Step 6: Check BIOS resume debug code,already entire process.
- Step 7: Check system whether back to OS working mode.
- Step 8: Load current chipset register setting to compare with old setting.

Thank You!